1

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

DTIC FILE COPY

AD-A214 277

# REPORT DOCUMENTATION PAGE

DTIC ELECTE NOV 13 1989 S B D

| | |
|---|---|
| 1a. REPORT SECURITY CLASSIFICATION<br>UNCLASSIFIED | 1b. RESTRICTIVE MARKINGS |
| 2a. SECURITY CLASSIFICATION AUTHORITY | 3. DISTRIBUTION/AVAILABILITY OF REPORT<br>Approved for public release; distribution is unlimited. |
| 2b. DECLASSIFICATION/DOWNGRADING SCHEDULE | |
| 4. PERFORMING ORGANIZATION REPORT NUMBER(S) | 5. MONITORING ORGANIZATION REPORT NUMBER(S) |
| 6a. NAME OF PERFORMING ORGANIZATION<br>Naval Ocean Systems Center | 6b. OFFICE SYMBOL (If applicable)<br>NOSC |
| 7a. NAME OF MONITORING ORGANIZATION | |
| 6c. ADDRESS (City, State and ZIP Code)<br>San Diego, California 92152-5000 | 7b. ADDRESS (City, State and ZIP Code) |
| 8a. NAME OF FUNDING/SPONSORING ORGANIZATION<br>Defense Advance Research Projects Agency | 8b. OFFICE SYMBOL (If applicable)<br>DARPA |
| 9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER | |
| 8c. ADDRESS (City, State and ZIP Code)<br>Office of Chief of Naval Research<br>1400 Wilson Blvd.<br>Arlington, VA 22209 | 10. SOURCE OF FUNDING NUMBERS |

| PROGRAM ELEMENT NO. | PROJECT NO. | TASK NO. | AGENCY ACCESSION NO. |
|---|---|---|---|
| 0602712E | EE13 | ONT | DN307 339 |

11. TITLE (include Security Classification)

A MODIFIABLE WEIGHT CIRCUIT FOR USE IN ADAPTIVE NEUROMORPHIC NETWORKS

12. PERSONAL AUTHOR(S)

P. A. Shoemaker and R. Shimabukuro

| 13a. TYPE OF REPORT | 13b. TIME COVERED | 14. DATE OF REPORT (Year, Month, Day) | 15. PAGE COUNT |
|---|---|---|---|
| presentation/paper | FROM TO | September 1989 | |

16. SUPPLEMENTARY NOTATION

| 17. COSATI CODES | | | 18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number) |
|---|---|---|---|
| FIELD | GROUP | SUB-GROUP | VHSIC/MIMIC<br>focused Ion Beam (FIB)<br>analog neural networks |

19. ABSTRACT (Continue on reverse if necessary and identify by block number)


The Naval Ocean Systems Center is involved in a collaborative effort with the Naval Weapons Center to implement neuromorphic networks in analog integrated circuitry using CMOS technology. We are investigating the use of a floating-gate charge storage device as a modifiable, non-volatile analog memory element for representing and storing interconnection weights between processing units, and have designed a simple circuit to sense this charge and perform the multiplicative "synaptic" function.

We employ the mechanism of avalanche or hot-carrier injection to move charge onto a floating-gate structure. This mechanism was first used in the mid-1970's for digital memory applications in the "FAMOS" (floating gate avalanche injection MOS) device, which consisted of a p-channel MOSFET with an isolated gate. At an appropriate biasing voltage, "hot" electrons are generated in avalanche breakdown, which have sufficient energy to conduct across the gate oxide and charge the gate. In an n-channel device, a complementary process takes place, with holes rather than electrons injected onto the floating gate. The potential due to the charge influences the state of the transistor under the gate just as would an externally applied voltage.

The memory cell which we have fabricated consists of two complementary pairs of transistors sharing a common floating gate. This configuration allows us to store an analog weight value, which may be increased with holes injected by an n-channel writing device, and decreased with electrons from a p-channel device (charges are mobile and free to recombine because the gate is a conductor). It is possible


(continued)

89 10 30 002

Published in *Neural Networks 1*. Supplement 1, 1988.

| | |
|---|---|
| 20. DISTRIBUTION/AVAILABILITY OF ABSTRACT<br>☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS | 21. ABSTRACT SECURITY CLASSIFICATION<br>UNCLASSIFIED |
| 22a. NAME OF RESPONSIBLE INDIVIDUAL<br>P. A. Shoemaker | 22b. TELEPHONE (Include Area Code)<br>(619) 553-5385 |
| 22c. OFFICE SYMBOL<br>Code 551 | |

19. ABSTRACT (Continued)

to increment or decrement the value by very small amounts by pulsing the writing voltages. The floating gate is surrounded by insulating silicon dioxide. This provides a very large energy barrier preventing charge leakage. From data reported in previous studies, we predict that values may be stored on the order of years.

Although in digital memories the same transistor which injects charge also senses its presence on the gate, in our circuits the gate is common to a second complementary pair of transistors, which perform the weighting function. These are depletion-mode devices (i.e., conducting at zero gate-to-source bias). The circuit in which they are used performs an approximate, four-quadrant multiplication, supplying an output current into virtual ground (as at the input node of a summing amplifier) which is roughly proportional to the product of the gate potential relative to ground, and an input signal.

We discuss in further detail experimental results obtained from test FAMOS and multiplier circuits fabricated at NOSC, control of the injection process and advantages and disadvantages of the FAMOS device, sources of error in the multiplier circuit, and the integration of the weight circuitry into neuromorphic systems.